WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory array including a plurality of memory cells, a plurality of word lines, a plurality of bit line pairs; and

a peripheral circuit including a decoder circuit which selects at least one memory cell in the memory array, driver circuits which drive the plurality of word lines to select levels, and a sense amplifier circuit which amplifies a potential on each of the bit line pair;

said each memory cell including a flip-flop circuit including a first inverter and a second inverter, and a pair of transmission MOS transistors respectively connected between the flip-flop circuit and the bit line pair connected to input/output nodes of the flip-flop circuit,

wherein an operating voltage of the memory cell and an operating voltage of the driver circuit are higher than an operating voltage of the decoder circuit, a threshold voltage of each MOS transistor included in the memory cell is higher than a threshold voltage of each MOS transistor included in the decoder circuit, a gate insulating film for the MOS transistors included in the memory cell is thicker than a gate insulating film for the MOS transistors included in the decoder circuit, and a selection level for the word line is higher than the level of the operating voltage of the decoder circuit.

2. The semiconductor memory device according to claim 1, wherein the ratio between a gate width and a gate length of each transmission MOS transistor included in the memory cell is identical to or set smaller than the ratio between a gate width and a gate length of each of N channel MOS transistors included in the first inverter and the second inverter.

3. The semiconductor memory device according to claim 1, wherein the ratio between a gate width and a gate length of a P channel load MOS transistor included in each of the first inverter and the second inverter is substantially identical to or set larger than the ratio between the gate width and gate length of each transmission MOS transistor included in the memory cell.

4. The semiconductor memory device according to claim 2, wherein a precharge level for the bit line pair is set lower than a selection level for the word line.

5. The semiconductor memory device according to claim 4, wherein the word-line selection level is set higher than a potential obtained by adding the threshold voltage of the transmission MOS transistor to the precharge level for the bit line pair, and the ratio between the gate width and gate length of the P channel load MOS transistor is greater than 0.9 times the ratio between the gate width and gate length of the transmission MOS transistor.

6. The semiconductor memory device according to claim 4, wherein the word-line selection level is set lower than a potential obtained by adding the threshold voltage of the transmission MOS transistor to the precharge level for the bit line pair, the ratio between the gage width and gate length of the P channel load MOS transistor is identical to or set smaller than the ratio between the gate width and gate length of the transmission MOS transistor, and the ratio between the gate width and gate length of the transmission MOS transistor is identical to or smaller than the ratio between the gate width and gate length of the N channel MOS transistor.

7. The semiconductor memory device according to claim 1, wherein the word-line selection level is the same potential as the operating voltage of the memory cell.

8. The semiconductor memory device according to claim 1, further including a step-up circuit which boosts a power supply voltage supplied from outside, wherein the memory cell and each of the driver circuits respectively use a voltage boosted by the step-up circuit as an operating voltage.